REMARKS

The Office Action dated November 18, 2003, has been received and carefully considered. In this response, claim 16 has been amended. Entry of the amendment to claim 16 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE INDEFINITENESS REJECTION OF CLAIMS 10-16

On page 2 of the Office Action, claims 10-16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the invention. This rejection is hereby respectfully traversed with amendment.

The Examiner asserts that claim 16 does not contain essential structural cooperative relationships between the claimed enabling circuit and other recited claim elements.

Claim 16 has been amended to address the concerns of the Examiner.

Regarding claims 10-15, it is respectfully submitted that these claims fully comply with the requirements of 35 U.S.C. § 112, second paragraph. Thus, it is respectfully submitted that

the aforementioned indefiniteness rejection of claims 10-15 is in error.

In view of the foregoing, it is respectfully requested that the aforementioned indefiniteness rejection of claims 10-16 be withdrawn.

II. THE ANTICIPATION REJECTION OF CLAIMS 1-9, 17-23, AND 33-39

On pages 2-4 of the Office Action, claims 1-9, 17-23, and 33-39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Coyle et al. (U.S. Patent No. 5,003,463). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed.

Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

The Examiner asserts that Coyle et al. teach the present invention as claimed. However, the Examiner fails to explain how Coyle et al. teach, or even suggest, how first data is transmitted from a first device to a second device and second data is transmitted from the second device to the first device, all simultaneously over a common bus. This feature is prevalent in claims 1-9, 17-23, and 33-39 of the present application and is supported throughout the specification. It is respectfully submitted that Coyle et al. fail to teach, or even suggest, such a feature. Accordingly, it is respectfully submitted that the present invention is not anticipated by Coyle et al..

The Examiner specifically asserts, with respect to claim 6, that Coyle et al. disclose a "system providing simultaneous bidirectional signaling using a bus topology, the system comprising: a first device (18/20 and SBI 0 or MCU 22, for example) operably coupled to a bus (SB 12); a second device (IOP 1 or MEM 0) operably coupled to the bus (SB 12), the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a first set of data ***[over the bus]*** to the second device (IOP

1 or MEM 0) and the second device (IOP 1 or MEM 0) transmitting a second portion of the first set of data ***[over the bus]*** to the first device (18/20 and SBI 0 or MCU 22) simultaneously during a first exchange slot; and a third device (IOP 2 or MEM 1, for example) operably coupled to the bus (SB 12), the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a second set of data ***[over the bus]*** to the third device (SBI 2 or MEM 1, for example) and the third device (SBI 2 or MEM 1, for example) transmitting a second portion of the second set of data ***[over the bus]*** to the first device (18/20 and SBI 0 or MCU 22, for example) simultaneously during a second exchange slot."
(omissions added)

First of all, Applicants respectfully submit that Coyle et al. do not in any way disclose a system for providing simultaneous bidirectional signaling on a common bus. Such simultaneous bidirectional signaling on a common bus as defined in the present application requires that at least two devices transmit data on the same bus at the same time. While it is clear to the Applicants that Coyle et al. do not claim, disclose, or even suggest such a system, it is apparently not as clear to the Examiner. To assist the Examiner in his understanding of the presently claimed invention, Applicants will now discuss additional differences between the presently

claimed invention and Coyle et al. which contradict the assertions of the Examiner.

Coyle et al. do not in fact teach that the "second device" (IOP 1 or MEM 0) is operably coupled to the bus (SB 12) (see first underlined passage above). In contrast, the "second device" (IOP 1 or MEM 0) is operably coupled to a totally separate local bus (IO BUS 42 or 43 or MEM BUS 24, respectively). It is also noted that the Examiner conveniently omitted the ***"over the bus"*** claim language in his comparison to Coyle et al. (see bold and italicized omissions above). Thus, it is clear that Coyle et al. do not in fact teach the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a first set of data ***over the bus*** to the second device (IOP 1 or MEM 0) and the second device (IOP 1 or MEM 0) transmitting a second portion of the first set of data ***over the bus*** to the first device (18/20 and SBI 0 or MCU 22) simultaneously during a first exchange slot.

Similarly, Coyle et al. do not in fact teach that the "third device" (IOP 2 or MEM 1) is operably coupled to the bus (SB 12) (see second underlined passage above). In contrast, the "third device" (IOP 2 or MEM 1) is operably coupled to a totally separate local bus (IO BUS 42 or 43 or MEM BUS 24, respectively). It is again also noted that the Examiner

conveniently omitted the ***"over the bus"*** claim language in his comparison to Coyle et al. (see bold and italicized omissions above). Thus, it is clear that Coyle et al. do not in fact teach the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a second set of data ***over the bus*** to the third device (SBI 2 or MEM 1, for example) and the third device (SBI 2 or MEM 1, for example) transmitting a second portion of the second set of data ***over the bus*** to the first device (18/20 and SBI 0 or MCU 22, for example) simultaneously during a second exchange slot."

In view of the foregoing, it is respectfully submitted that Coyle et al. fail to claim, disclose, or even suggest the recited features of claim 6. Accordingly, it is respectfully submitted that claim 6 is not anticipated by Coyle et al..

The arguments discussed above with respect to claim 6 may also be applied to any of independent claims 1, 17, 33, and 39. Thus, it is respectfully submitted that claims 1, 17, 33, and 39 are also not anticipated by Coyle et al..

Regarding claims 2-5, 7-9, 18-23, and 34-38, these claims are dependent upon independent claims 1, 6, 17, and 33, respectively. Since independent claims 1, 6, 17, and 33 should be allowable as discussed above, dependent claims 2-5, 7-9, 18-23, and 34-38 should also be allowable at least by virtue of

their dependency on independent claims 1, 6, 17, and 33. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 7 recites that a turnaround delay exists between the first exchange slot and the second exchange slot. The Examiner asserts that there is always a delay in memory access. However, nowhere do Coyle et al., or any of the other cited references teach a turnaround delay between simultaneous bidirectional transmissions on a common bus, as presently claimed. Thus, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify where such a turnaround delay is taught.

Also, claim 8 recites that the turnaround delay is less than twice an end-to-end propagation delay of the bus. The Examiner asserts that it is clear that in Coyle et al., due to simultaneous transferring and buffers, the so-called "turnaround delay" is less than twice an end-to end propagation delay of the bus. However, as discussed above, Coyle et al. do not claim, disclose, or even suggest simultaneous bidirectional transmissions on a common bus. Thus, Coyle et al. also do not claim, disclose, or even suggest that the turnaround delay between simultaneous bidirectional transmissions on a common bus

is less than twice an end-to-end propagation delay of the common bus, as presently claimed. Thus, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify where such a turnaround delay is taught.

At this point, the Applicants would like to address the assertion made by the Examiner that "during patent examination, the pending claims must be given the broadest reasonable interpretation consistent with the specification." Applicants agree with this assertion. Indeed, when the present pending claims are given the broadest reasonable interpretation consistent with the specification, it is still clear that Coyle et al. do not teach the claimed limitations. In the simplest terms, Coyle et al. do not claim, disclose or even suggest a system or method wherein simultaneous bidirectional signaling is performed on a common bus. Thus, it is respectfully submitted that claims 1-9, 17-23, and 33-39 are not anticipated by Coyle et al.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-9, 17-23, and 33-39 be withdrawn.

III. <u>THE ANTICIPATION REJECTION OF CLAIMS 10-16 AND 24-32</u>

On pages 4-5 of the Office Action, claims 10-16 and 24-32 were rejected under 35 U.S.C. § 102(e) as being anticipated by Tamura et al. (U.S. Patent No. 6,493,394). This rejection is hereby respectfully traversed.

The Examiner asserts that Tamura et al. teach the present invention as claimed. However, the Examiner fails to explain how Tamura et al. teach, or even suggest, simultaneous bidirectional signaling on a common bus in any manner. This feature is prevalent in claims 10-16 and 24-32 of the present application and is supported throughout the specification. It is respectfully submitted that Tamura et al. fail to teach, or even suggest, such a feature. In fact, Tamura et al. teach away from such a feature by indicating that the conditions associated with such a feature would result only from an error (see column 41, lines 11-16). Accordingly, it is respectfully submitted that the present invention is not anticipated by Tamura et al..

The Examiner specifically asserts, with respect to claim 10, that Tamura et al. discloses a device coupled to a bus in a bus topology for providing simultaneous bi-directional signaling, the device comprising: a driver (201/301, for example) configured to provide additive signaling, the driver applying transmit signals to the bus (202/302, for example); a receiver circuit (shown in Fig. 12 or 13, for example) operably

coupled to the driver, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot.

First of all, Applicants respectfully submit that Tamura et al. do not in any way disclose a system for providing simultaneous bidirectional signaling on a common bus. Such simultaneous bidirectional signaling on a common bus as defined in the present application requires that at least two devices transmit data on the same bus at the same time. While it is clear to the Applicants that Tamura et al. do not claim, disclose, or even suggest such a system, it is apparently not as clear to the Examiner. To assist the Examiner in his understanding of the presently claimed invention, Applicants will now discuss additional differences between the presently claimed invention and Tamura et al. which contradict the assertions of the Examiner.

Tamura et al. do not in fact teach that the driver (201/301, for example) is configured to provide additive signaling (see first underlined passage above). In contrast, the "driver" (201/301, for example) is merely a single-ended driver for driving a transmission line (see column 25, line 16 through column 26, line 43; Figures 7 and 9). Nowhere do Tamura

et al. describe the "driver" (201/301, for example) as providing additive signaling.

Tamura et al. also do not in fact teach that the receiver circuit (shown in Fig. 12 or 13, for example) is configured to effectively subtract the transmit signals to receive received signals from the bus (see second underlined passage above). In contrast, the "receiver circuit" (shown in Fig. 12 or 13, for example) is merely a single-ended receiver for receiving signals from a transmission line (see column 27, line 16 through column 28, line 20; Figures 12 and 13). Nowhere do Tamura et al. describe the "receiver circuit" (shown in Fig. 12 or 13, for example) as being configured to effectively subtract the transmit signals to receive received signals from the bus. In fact, Tamura et al. do not even disclose the "receiver circuit" (shown in Fig. 12 or 13, for example) being operably coupled to the "driver" (201/301, for example).

In view of the foregoing, it is respectfully submitted that Tamura et al. fail to claim, disclose, or even suggest the recited features of claim 10. Accordingly, it is respectfully submitted that claim 10 is not anticipated by Tamura et al..

The arguments discussed above with respect to claim 10 may also be applied to independent claims 24 and 28. Thus, it is

respectfully submitted that claims 24 and 28 are also not anticipated by Tamura et al..

Regarding claims 11-16, 25-27, and 29-32, these claims are dependent upon independent claims 10, 24, and 28, respectively. Since independent claims 10, 24, and 28 should be allowable as discussed above, dependent claims 11-16, 25-27, and 29-32 should also be allowable at least by virtue of their dependency on independent claims 10, 24, and 28. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 11 recites that the device is coupled to the bus by an impedance-matching splitter. The Examiner asserts that it is clear that each memory device is connected to the bus (transmission line) by its own impedance matching. However, nowhere do Tamura et al., or any of the other cited references, teach that the device is coupled to the bus by an impedance-matching splitter, as presently claimed. Thus, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, specifically identify where this claimed feature is taught.

Also, claim 12 recites that the device comprises a terminator operably coupled to the driver and the receiver

circuit, wherein the terminator provides a controlled termination impedance. The Examiner asserts that a terminator (761, 762, for example) operably is coupled to the driver and the receiver circuit, the terminator providing a controlled termination impedance. However, the terminators (761, 762, for example) disclosed by Tamura et al. are separate active terminators (see column 42, lines 4-32; Figures 40A and 40B), and are not part of any device having a driver and a receiver circuit, as presently claimed. Thus, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, specifically identify where this claimed feature is taught.

Also, claim 13 recites that the device comprises a transmit circuit operably coupled to the driver, wherein the transmit circuit comprises a transmit buffer, wherein the transmit buffer holds data pending arrival of the exchange slot. The Examiner asserts that the signal transmission system (including buffers, 708, for example) of Tamura et al. is readable as "transmit circuit." However, the buffers 708 disclosed by Tamura et al. are buffers between signal lines (see column 40, lines 1-15; Figure 34), and are not transmit buffers for holding data pending arrival of an exchange slot, as presently claimed. Thus, Applicants respectfully request that the Examiner, in

accordance with his duty to present at least a prima facie case of anticipation, specifically identify where this claimed feature is taught.

Also, claim 14 recites that the transmit buffer comprises a plurality of transmit buffers, wherein the plurality of transmit buffers are configured to hold data destined for different other devices. The Examiner asserts that the device of Tamura et al. also includes buffering stages (buffers 708, for example) or "a plurality of transmit buffers." However, the buffers 708 disclosed by Tamura et al. are for providing signal delays (see column 40, lines 1-15; Figure 34), and are not a plurality of transmit buffers configured to hold data destined for different other devices, as presently claimed. Thus, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, specifically identify where this claimed feature is taught.

Also, claim 15 recites that the receiver circuit comprises a comparator operably coupled to the transmitter and to the driver, wherein the comparator is configured to effectively subtract the transmit signals to yield received signals from the bus. The Examiner asserts that Tamura et al disclose a receiver circuit comprising a comparator (713, for example) operably coupled to the transmitter and to the driver and the receiver.

However, the comparator 713 disclosed by Tamura et al. is a phase comparator (see column 41, lines 17-49; Figure 38), and is not a comparator configured to effectively subtract the transmit signals to yield received signals from the bus, as presently claimed. Thus, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, specifically identify where this claimed feature is taught.

Also, claim 16 recites an enabling circuit, coupled to the transmit circuit and the receive circuit, responsive to an exchange slot indication, wherein the enabling circuit enables the operation of the transmit circuit and the receive circuit during the exchange slot. The Examiner asserts that it is clear from the drawings and disclosure of Tamura et al. that the operations of the transmission system and receiver circuit must be enabled by some circuit means during exchange slot. However, it is respectfully submitted that it is not clear to the Applicants, nor anyone else for that matter, how Tamura et al. disclose an enabling circuit, coupled to the transmit circuit and the receive circuit, responsive to an exchange slot indication, wherein the enabling circuit enables the operation of the transmit circuit and the receive circuit during the exchange slot, as presently claimed. Thus, Applicants

respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, specifically identify where this claimed feature is taught.

In view of the foregoing, it is respectfully submitted that the aforementioned anticipation rejection of claims 10-16 and 24-32 is improper, and the withdrawal of such rejection is respectfully requested.

IV. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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APPENDIX A

1 (Original). A method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of:

selecting a first device and a second device from among a plurality of devices operably coupled to a common bus to exchange a first set of data;

scheduling a first exchange slot over which the first device and the second device are to exchange the first set of data; and

during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first device to the second device over the common bus and transmitting a second portion of the first set of the data from the second device to the first device over the common bus.

2 (Original). The method of claim 1 further comprising the steps of:

selecting the first device and a third device to exchange a second set of data;

scheduling a second exchange slot over which the first device and the third device are to exchange the second set of data; and

during the second exchange slot, simultaneously

transmitting a first portion of the second set of data from the first device to the third device over the common bus and transmitting a second portion of the second set of the data from the third device to the first device over the common bus.

3 (Original). The method of claim 2 further comprising the step of:

introducing a turnaround delay between the first exchange slot and the second exchange slot.

4 (Original). The method of claim 3 wherein the turnaround delay is less than twice an end-to-end propagation delay of the common bus.

5 (Original). The method of claim 1 wherein the first device is a memory controller, and the second device is a memory device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

6 (Previously Presented). A system providing simultaneous bidirectional signaling using a bus topology, the system

comprising:

a first device operably coupled to a bus;

a second device operably coupled to the bus, the first device transmitting a first portion of a first set of data over the bus to the second device and the second device transmitting a second portion of the first set of data over the bus to the first device simultaneously during a first exchange slot; and

a third device operably coupled to the bus, the first device transmitting a first portion of a second set of data over the bus to the third device and the third device transmitting a second portion of the second set of data over the bus to the first device simultaneously during a second exchange slot.

7 (Original). The system of claim 6 wherein a turnaround delay exists between the first exchange slot and the second exchange slot.

8 (Original). The system of claim 7 wherein the turnaround delay is less than twice an end-to-end propagation delay of the bus.

9 (Original). The system of claim 6 wherein the first device is a memory controller, and the second device is a memory device

and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

10 (Previously Presented). A device coupled to a bus in a bus topology for providing simultaneous bidirectional signaling, the device comprising:

a driver configured to provide additive signaling, the driver applying transmit signals to the bus;

a receiver circuit operably coupled to the driver, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot.

11 (Original). The device of claim 10 wherein the device is coupled to the bus by an impedance-matching splitter.

12 (Original). The device of claim 10 wherein the device further comprises:

a terminator operably coupled to the driver and the receiver circuit, the terminator providing a controlled termination impedance.

13 (Original). The device of claim 10 wherein the device further comprises:

a transmit circuit operably coupled to the driver, the transmit circuit comprising a transmit buffer, the transmit buffer holding data pending arrival of the exchange slot.

14 (Previously Presented). The device of claim 13 wherein the transmit buffer further comprises:

a plurality of transmit buffers, the plurality of transmit buffers configured to hold data destined for different other devices.

15 (Previously Presented). The device of claim 13 wherein the receiver circuit further comprises:

a comparator operably coupled to the transmitter and to the driver, the comparator configured to effectively subtract the transmit signals to yield received signals from the bus; and

a receiver operably coupled to the comparator, the receiver receiving the received signals and obtaining received data from the received signals.

16 (Currently Amended). The device of claim 15 further

comprising:

an enabling circuit, coupled to the transmit circuit and the receive circuit, responsive to an exchange slot indication, the enabling circuit enabling the operation of the transmit circuit and the receive circuit during the exchange slot.

17 (Previously Presented). A memory system comprising:

a memory controller;

a bus operably coupled to the memory controller;

a first memory device operably coupled to the bus, the first memory device configured to simultaneously send first read data to the memory controller via the bus and receive first write data from the memory controller via the bus; and

a second memory device operably coupled to the bus, the second memory device configured to simultaneously send second read data to the memory controller via the bus and receive second write data from the memory controller via the bus.

18 (Previously Presented). The memory system of claim 17 wherein the first memory device is configured to simultaneously send the first read data to the memory controller and receive the first write data from the memory controller during a first exchange slot and wherein the second memory device is configured

to simultaneously send the second read data to the memory controller and receive the second write data from the memory controller during a second exchange slot.

19 (Original). The memory system of claim 18 wherein the memory controller comprises:

a first write buffer to hold the first write data pending arrival of the first exchange slot.

20 (Original). The memory system of claim 19 wherein the memory controller comprises:

a second write buffer to hold the second write data pending arrival of the second exchange slot.

21 (Previously Presented). The memory system of claim 17 wherein the bus comprises:

a conductor operably coupling the first memory device and the second memory device to the memory controller, wherein the first memory device is configured to simultaneously send a first read bit of the first read data to the memory controller over the conductor and receive a first write bit of the first write data from the memory controller over the conductor during a first exchange slot and wherein the second memory device is

configured to simultaneously send a second read bit of the second read data to the memory controller over the conductor and receive a second write bit of the second write data from the memory controller over the conductor during a second exchange slot.

B

22 (Original). The memory system of claim 21 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

23 (Original). The memory system of claim 17 wherein the memory controller performs coherency checking during memory access operations.

24 (Previously Presented). A memory device comprising:

a driver configured to drive a bus with read data during an exchange slot while write data are present on the bus;

a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the write data from the bus during the exchange slot while the driver is driving the bus with the read data; and

a memory circuit operably coupled to the receiver circuit,

the memory circuit configured to provide the read data and to store the write data.

25 (Previously Presented). The memory device of claim 24 further comprising:

an enabling circuit responsive to an exchange slot indication, the enabling circuit operably coupled to the driver and the receiver circuit, the enabling circuit enabling interaction of the driver and the receiver circuit with the bus during the exchange slot.

26 (Previously Presented). The memory device of claim 25 wherein the enabling circuit is configured to be responsive to the exchange slot indication following a turnaround delay sufficient to prevent inter-symbol interference.

27 (Original). The memory device of claim 24 further comprising:

a transmit circuit operably coupled to the driver, the transmit circuit comprising a transmit buffer, the transmit buffer holding the read data pending arrival of the exchange slot.

28 (Previously Presented). A memory controller comprising:

a driver configured to drive a bus with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device are present on the bus;

a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the first read data from the bus during the first exchange slot while the driver is driving the bus with the first write data.

29 (Previously Presented). The memory controller of claim 28 wherein the driver is further configured to drive the bus with second write data destined for a second memory drive during a second exchange slot while second read data from the second memory device are present on the bus and wherein the receiver circuit is further configured to receive the second read data from the bus during the second exchange slot while the driver is driving the bus with the second write data.

30 (Original). The memory controller of claim 29 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

31 (Original). The memory controller of claim 28 further comprising:

a transmit circuit operably coupled to the driver to transmit the first write data and the second write data to the driver, the transmit circuit comprising a transmit buffer to hold the first write data pending arrival of the first exchange slot and the second write data pending arrival of the second exchange slot.

32 (Original). The memory controller of claim 31 wherein the transmit buffer comprises:

a first transmit buffer to hold the first write data pending arrival of the first exchange slot; and

a second memory buffer to hold the second write data pending arrival of the second exchange slot.

33 (Original). A method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of:

during a first exchange slot, simultaneously communicating over a common bus first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory

controller; and

during a second exchange slot, simultaneously communicating over a common bus second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller.

B

34 (Original). The method of claim 33 further comprising the step of:

holding the first write data destined for the first memory device in the memory controller pending arrival of the first exchange slot.

35 (Original). The method of claim 34 further comprising the step of:

holding the second write data destined for the second memory device in the memory controller pending arrival of the second exchange slot.

36 (Original). The method of claim 35 wherein the step of holding the first write data occurs in a first write buffer and wherein the step of holding the second write data occurs in a second write buffer.

37 (Original). The method of claim 35 further comprising the steps of:

holding the first read data destined for the memory controller in the first memory device; and

holding the second read data destined for the memory controller in the second memory device.

38 (Original). The method of claim 37 wherein the step of simultaneously communicating over the common bus the first write data from the memory controller to the first memory device and the first read data from the first memory device to the memory controller occurs after a specified amount of the first write data destined for the first memory device is hold in the memory controller.

39 (Previously Presented). A system for bidirectional communication of data over a common bus comprising:

a first device operably coupled to the common bus, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit buffer to hold first-to-third data;

a second device operably coupled to the common bus, the

second device comprising a second-to-first transmit buffer to hold second-to-first data;

a third device operably coupled to the common bus, the third device comprising a third-to-first transmit buffer to hold third-to-first data; and

a scheduler operably coupled to the common bus, the scheduler scheduling the first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus simultaneously during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-first data over the common bus simultaneously during a second exchange slot, the scheduler introducing a turnaround delay sufficient to prevent inter-symbol interferences between the first exchange slot and the second exchange slot.